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MISSILE X PROTECTIVE SHELTER C(3) PROCESSOR STUDY REPORT,(U)
DEC 80 S R RANE F04704-80-C-0018

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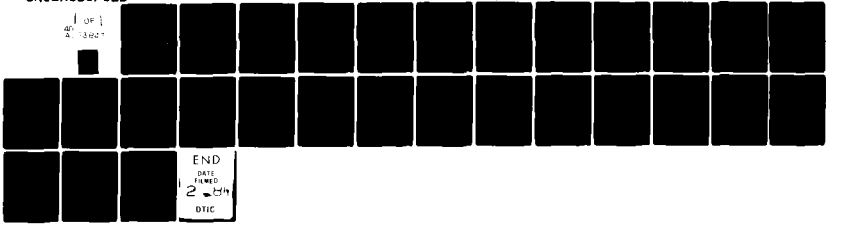

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Z80 As HSS Processor
DMA Vs Program I/O
COMSEC for HSS

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Use of an 8-bit microprocessor such as Z80 for HSS processing tasks. Advantage of program I/O Vs DMA in such application. Prediction figures of high reliability and low power dissipation for such approach. Analysis of dual processor architecture to separate red and black data.

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MISSILE X
PROTECTIVE SHELTER C^3
PROCESSOR STUDY REPORT
1 December 1980

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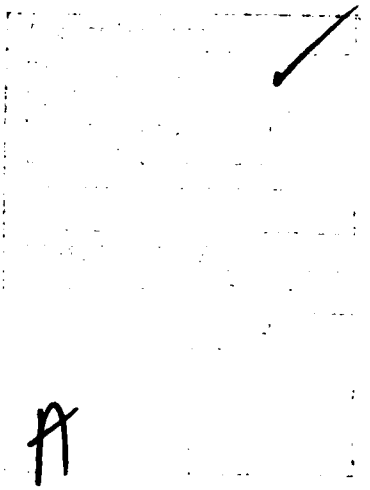
PREFACE

This study was originally undertaken to demonstrate that there were viable LSI alternatives to low power schottki T^2L solutions for M-X C^3 HSS applications. During the course of this effort, GTE Sylvania was apprised of the study and conclusions - they have subsequently reached similar conclusions, and with BMO's concurrence have baselined eight-bit LSI architecture for HSS applications.



HSS COMMUNICATION CONTROLLER

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1.0 SCOPE

This study will show that an 8-bit microprocessor such as the Z80 is ideal for HSS processing tasks. Furthermore, by comparing DMA and Program I/O execution times, it is shown that the use of DMA does not enhance the HSS processor's processing capability. The NSA suggested dual processor architecture is analyzed to show the impact on reliability, power and cost.

2.0 OBJECTIVES

The following objectives were considered in the design of this processor:

1. High Reliability
2. Low Power Consumption
3. Low Life Cycle Cost

   If the hardware is kept to a minimum, it will have significant impact on the above three objectives. This is the basic goal for this study.

2.1 Ground Rules

1. Considering the F/O cables and the other interfaces as I/O devices, the most important functions of the microprocessor will be to handle the data to and from these devices. Thus, the selected microprocessor's architecture should have powerful I/O handling capability.
2. The microprocessor must be a qualified MIL-M-38510 part or in the process of being qualified.

2.1 Ground Rules (continued)

3. The microprocessor should be widely used in industry. This is important for:
   1) Cost is reduced
   2) Provides multiple sources
   3) A good number of peripheral devices are available
   4) Reliable software development tools are available from several sources.
4. A CMOS version of NMOS microprocessor with CMOS support-chips is considered to point out the impact on power dissipation. Even if such a device is not currently available, NMOS version could be used for development and later substituted with CMOS.
5. 8-bit architecture with 16-bit internal registers is considered to keep the hardware to minimum. An unavoidable compromise one must make when one squeezes a 16-bit CPU into a 40 pin DIP package is moving both data and addresses in and out of the CPU on the same 16-bit bus. One cannot have the separate address and data buses that have become standard in 8 bit machines. This does not necessarily cost operating speed because rarely would the address and data flow at the same time in a computer, but it does cost extra parts for latching.

3.0 SUMMARY

Included in This Report

- Description of HSS Communications controller
- Advantages of using Z80 for this application
- Comparison between DMA and program I/O
- Alternate dual microprocessor architecture to isolate red and black data
- Reliability predictions
- Power dissipation comparison between low power schottky (+ Some NMOS) and CMOS components

3.0 (continued)

Conclusions

- o Z80 is the best 8-bit microprocessor for HSS application that is currently available.
- o No need of DMA.
- o High reliability can be achieved using NMOS components.
- o Power dissipation significantly lower than baseline. Even lower power dissipation could be achieved by using CMOS.

Recommendations

- o Use Z80 microprocessor for HSS processing
- o Eliminate DMA

4.0 DOCUMENTATION

1) ZILOG Z80-CPU technical manual

2) ZILOG Z80-CTC technical manual

3) AMD data sheet on 2661

4) GTE alternate processor implementation study

5) An introduction to microcomputers Vol II by A. Osborne

5.0 PROCESSOR ARCHITECTURE

Description of HSS Communication Controller (Reference Figure 1)

Serial data coming via fiber optic modem is converted to TTL compatible levels by fiber optic interface circuits. The serial data is transformed into a byte format by the USART.* As the data transfer rate is 48Kbaud/sec., each bit arrives at the USART at 20.83 μSec intervals. The USART provides double buffering (2, 8-bit registers). The first buffer of the USART will be full after 166.66 μSec, then the USART will raise "receiver ready" flag. This signal is used to advance the counter which is keeping count

*USART (Universal Synchronous Asynchronous Receiver Transmitter) In addition, the USART handles all control protocol between the modem and the CPU.

5.0 (continued)

of th number of bytes received. This signal is also used by the FIFO (First In-First Out buffer) to extract the byte from the USART and store it in its register. It takes 1 msec (166.66 X 6 μSec) to store 6 bytes in the FIFO. When the 6th byte is stored in the FIFO, the counter interrupts the CPU. The interrupt service routine (fig. 2, & table 1) which is stored in the PROM, transfers the 6 bytes of data from FIFO to specified locations in RAM. It takes the Z80, 212 clock cycles or 53.0 μSec, with the Z80 clock running at 4 Mhz, to transfer the six bytes. Thus, the processor takes only 5.3% of the total time required to receive the 6 bytes at 48K baud transfer rate. It should be noted that as the data is transferred to RAM, it does not exist anymore in the FIFO. The 57401 has an architecture to store 16X4 bits and thus 2 chips will store 16 bytes of data. Though the CPU is interrupted after every 6 bytes, there is not great urgency for the CPU to transfer the data as it has (166.66x10μS)1.66 msec to respond before the FIFO is full. In other words, the CPU can go through an interrupt service routine about 6000 clock cycles long without losing any data. The first word (6 bytes) is processed as shown in the flow chart. (Figure 3)

When the decision is made to retransmit the data in a specified direction, the CPU bypasses the FIFO and sends the data one byte at a time to the selected USART.

When the CPU is not servicing an interrupt or processing data, it can poll the interface devices, format a status word and transmit.

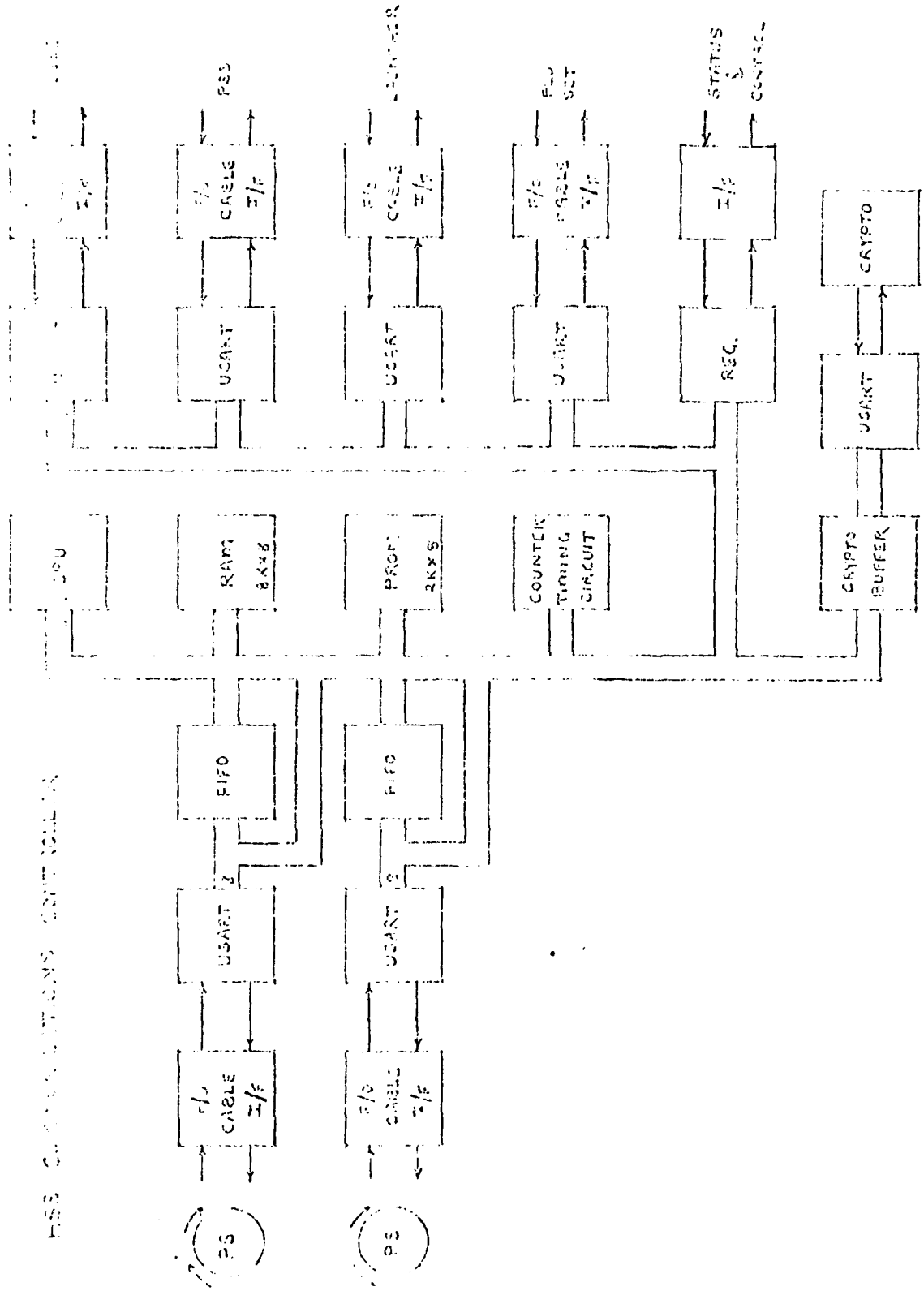
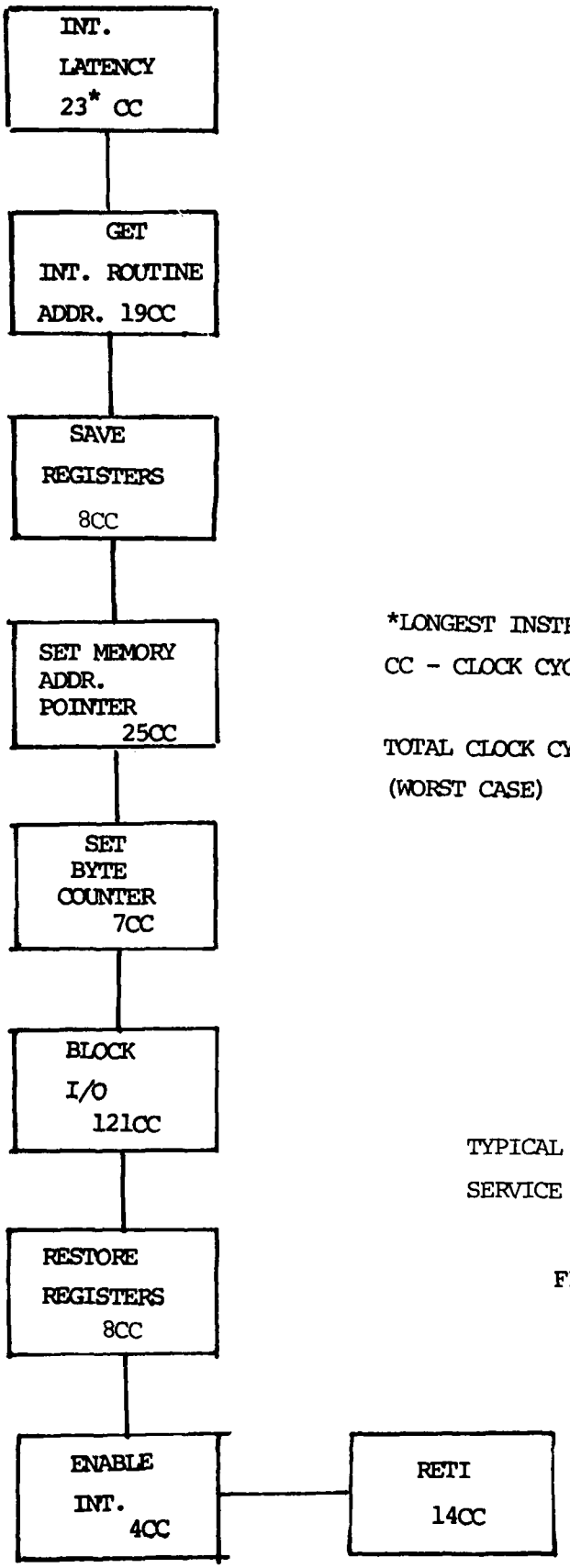

CRYPTO
USART
REG.
STATUS
&
CONTROL
USART
CRYPTO
BUFFER
COUNTER
TIMING
CIRCUIT
PROM
2K X 8
RAM
2K X 8
CPU
FIFO
FIFO
USART
USART
CABLE
T/R
CABLE
T/R
PS
PS

FIG 1



*LONGEST INSTRUCTION

CC - CLOCK CYCLE

TOTAL CLOCK CYCLES = 229
(WORST CASE)

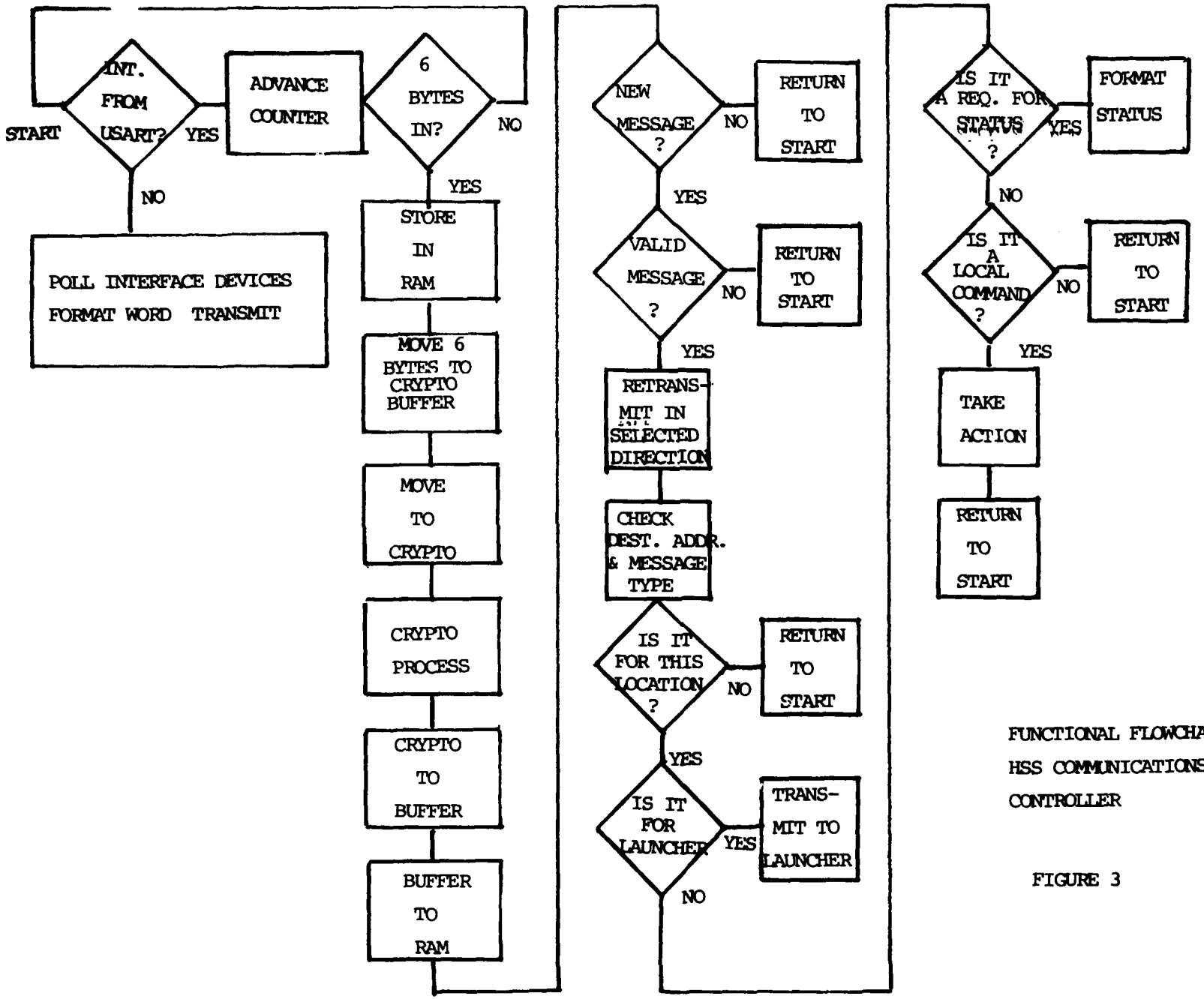
TYPICAL INTERRUPT
SERVICE FLOW CHART

FIGURE 2

INTERRUPT SERVICE ROUTINE TO TRANSFER 6 BYTES FROM FIFO TO RAM

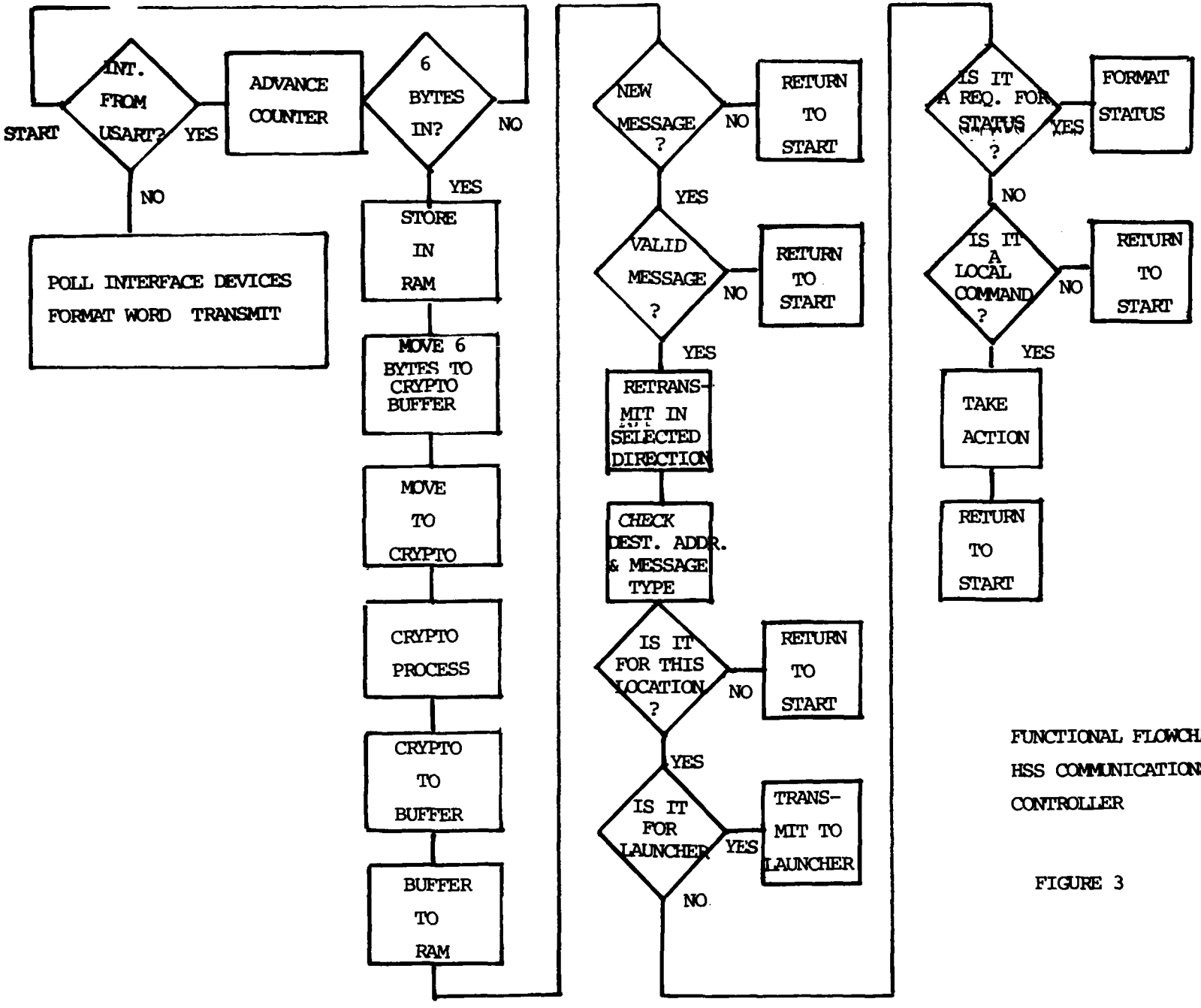
Comments	Instruction	Clock Cycles	Execution Time(μS)
Save Registers & Flags	EXX AF	4	1.00
	EXX	4	1.00
Memory Location	PUSH IX	15	3.75
Use HL as Addr. Pointer	POP HL	10	2.5
Load Byte Counter	LD B.6	7	1.75
In FIFO	INIR	121	30.25
	Push HL	11	2.75
	Pop IX	14	3.5
Restore Registers and Flags	Ex AF	4	1.0
	EXX	4	1.0
Enable Int.	ENI	4	1.0
Return from Int.	RETI	14	3.5
	Total	212	53.0

TABLE I.



FUNCTIONAL FLOWCHART
HSS COMMUNICATIONS
CONTROLLER

FIGURE 3



FUNCTIONAL FLOWCHART
HSS COMMUNICATIONS
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FIGURE 3

6.0 Selection of Microprocessor

Desirable hardware objectives are a single power supply (+5v), and a single system clock signal.

The following Z80 unique features are not found in 8080, 8085, 6809 with some exceptions: The standard general purpose registers and status flags have been duplicated. This makes it very easy to handle single-level interrupts. General purpose register and accumulator contents no longer need to be saved on the stack, instead the program may simply switch to the alternate register set. At any time, one or the other set of registers, but not both, are accessible. There are two index registers which makes indexed memory addressing easier.

Z80 interrupt knowledge logic gives the option of initiating an interrupt service rountine with a call instruction, where the high order address byte for the call is provided by the interrupt vector register. The 8085 also provides this capability.

The memory refresh counter register represents a feature of microcomputer systems which have been overlooked by everyone except Fairchild and Zilog. Dynamic memory devices will not hold their contents for very long, irrespective of whether power is off or on. A dynamic memory must therefore be accessed at milli-second intervals. Dynamic memory devices compensate for this short-coming by being very inexpensive. Using a technique similar to direct

6.0 Selection of Microprocessor (continued)

memory access, dynamic refresh circuitry will periodically access dynamic memories, rewriting the contents of individual memory words on each access. About the only logic needed by dynamic refresh is a counter via which it keeps track of its progress through the dynamic memory; that is the purpose of the Z80 memory refresh counter register. The Z80 also has a special DMA refresh control signal; therefore, the Z80 provides all necessary dynamic refresh logic. Thus, it is easier and inexpensive to incorporate dynamic memories with Z80.

The Z80 addressing enhancements are of significant value when comparing the Z80 to the 8080A. The value of the index register comes not so much from having an additional addressing option, but rather two 16-bit index registers allow a programmer to manage his CPU register space more effectively. Look upon these index registers as performing memory addressing tasks which the 8080A would have to perform using the general purpose registers. By freeing up these registers for data manipulation, one can significantly reduce the number of memory reference instructions executed by the Z80.

Block Transfer I/O Instructions. These instructions move a block of data between the I/O port identified by register C and a memory location addressed by the H and L register pair. Register B is used as a block byte counter. After each byte of data within the block is transferred, the contents of register B are decremented; one can specify block transfer I/O instructions that will either increment or decrement the memory address in registers H and L. Here is a programming example with the 8080A equivalent:

6.0 Selection of Microprocessor (continued)

For Storing 6 bytes:

Z80

INSTRUCTION				CLOCK CYCLES
LD B, COUNT				7
LD C, PORTN				7
LD HL, START LOOP				10
OTIR	21(16 when B=0)	21x5	=	105
		16x1	=	16
				145

At 4 MHz Clock ≡ 36.25μSec

8080A

	INSTRUCTION			CLOCK CYCLES
	MVI B, COUNT			10
	LXI H, START			10
Loop:	IN PORTN	10		
	MOV M, A	7		
	INX H	5	X6 =	222
	DCR B	5		
	JNZ ;Loop	10		
		For 6 bytes.		242

At 4 MHz ≡ 60.5 μSec

6.0 Selection of Microprocessor (continued)

These instruction sequences input COUNT bytes from I/O port PORTN, and store the data in a memory buffer whose beginning address is START. COUNT and PORTN are symbols representating 8-bit numbers. START is an address label. The block transfer I/O instruction will continue executing until the B register has decremented to 0.

Advantages Gained by having the Z80 I/O Instructions. The value of the register indirect I/O instructions is that programs stored in ROM can access any I/O port. If I/O port assignments change, then all one needs to do is modify that small portion of program which loads the I/O port address into the C register.

In response to the execution of a single instruction object code up to 256 bytes of data may be transferred between memory and I/O port. This data transfer occurs at CPU speed - which means external logic must input or output data at the same speed.

A memory block transfer instruction allows one to move up to 64K bytes of data between two memory buffers which may be anywhere in memory. One can use BLOCK MOVE instructions in Z80 configurations that include dynamic memory. While the BLOCK MOVE is being executed, dynamic memory is refreshed.

The BLOCK SEARCH instruction will search a block of data in memory looking for a match with the accumlator contents. This instruction is particularly useful when searching a large memory buffer for a byte that may frequently occur.

6.0 Selection of Microprocessor (continued)

Bit Manipulation Instructions: Bit manipulations instructions are particularly important for signal processing. The Z80 has instructions that set to 1 (SET), reset to 0 (RES) or test (BIT) individual bits in memory or any general purpose register.

8085

The 8085 instruction set is almost identical to the 8080A instruction set; in contrast, the Z80 has a massively expanded instruction set. The large Z80 instruction set has been criticized for its complexity, but one could argue that since the Z80 also provides the complete 8080A instruction set, anyone who does not want to use the additional instructions can simply ignore them.

The 8085 multiplexes its Data Bus with the address bus lines. Such multiplexing demands other support devices, or external demultiplexing logic.

Microprocessor Instruction Time Analysis

A table of microprocessor instruction times for the GTE proposed microcomputer and eight other microprocessors was provided by GTE in their Alternate Processor Implementation Study. This table was extended (Table II) to accommodate Z80. From this table, it is clear that Z80 has a better throughput than the proposed microcomputer and 8086.

7.0 LSI SUPPORT CHIPS

USART (Universal Synchronous Asynchronous Receiver Transmitter)

2661 is a universal synchronous/asynchronous data communications controller chip. It interfaces directly to most 8-bit microprocessors and may be used in a polled or interrupt driven system environment. The 2661 accepts programmed instructions from the microprocessor while supporting many serial data communications disciplines - synchronous and asynchronous - in the full or half-duplex mode. The 2661 serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data character for input to the microprocessor. The 2661 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. The transmitter and receiver are doubled buffered and there is provision for local or remote maintenance loop back mode.

Operational Description: A set of control words must be sent to 2661 to define the desired mode and communications format. The control words will specify the baud rate factor (1X, 16X, 64X, character length (5 to 8), asynchronous or synchronous mode, etc. After receiving the control words, the 2661 is ready to communicate. 'Transmitter Ready' (TXRDY) is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TXRDY is automatically reset. Concurrently, 2661 may receive serial data; and after receiving an entire character, the 'Receiver Ready' (RXRDY) output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RXRDY.

TABLE II

MICROPROCESSOR INSTRUCTION TIME ANALYSIS

PROCESSOR	INTERNAL	EXTERNAL	INSTRUCTION CYCLE (5) (u SEC)	AVERAGE INSTRUCTION (1) (u SEC)	NORMALIZED AVERAGE INSTRUCTION (2) (u SEC)
DEC LSI 11	16 BIT	16 BIT	.350	6.68	12.23
PROPOSED u-COMPUTER	16 BIT	16 BIT		2.73	5
8086 (3)	16 BIT	16 BIT	.200	3.49	6.39
			.500	8.73	15.89
68000	16 BIT	16 BIT	.125	2.21	4.04
			.500	8.82	16.15
9900	16 BIT	16 BIT	.333	3.10	5.67
8088 (3)	16 BIT	8 BIT	.200	3.49	6.39
			.500	8.73	15.98
6809	16 BIT	8 BIT	1.00	5.75	10.53
8080A (4)	8 BIT	8 BIT	.48	11.42	20.92
			2.00	47.6	87.18
6800 (4)	8 BIT	8 BIT	.50	4.66	8.53
			.666	6.20	11.53
			1.00	9.30	17.03
1802 (4)	8 BIT	8 BIT	1.25	6.76	12.38
Z80(6)	16 BIT	8 BIT	0.250	2.51	4.6

(1) USED SOLOMON MIX

(2) NORMALIZED TO NORDEN INSTRUCTION MIX (FACTOR 1.8315)

(3) 8086 AND 8088 USE SAME INSTRUCTION SET

(4) FACTOR OF 2 APPLIED TO 8-BIT PROCESSORS EXCEPT Z80 TO NORMALIZE 16 BIT OPERATIONS.

(5) INSTRUCTIONS ARE GENERALLY MULTIPLE.

(6) 16-BIT GROUP INSTRUCTIONS ARE USED THEREFORE FACTOR OF 2 IS NOT APPROPRIATE.

7.0 USART (continued)

The Z80 Clock Timer Circuit (CTC):

The Z80 clock timer circuit is a programmable device which contains four sets of timing logic. Each set of timing logic can be programmed independently as an interval timer or an external event counter.

The master Z80 system clock is used by interval timer logic. A time out may be identified by an interrupt request.

An external signal such as an interrupt from USART is used to decrement when logic is functioning as an event counter. An interrupt may be requested when the predetermined number of events count out (such as 6 bytes in FIFO).

8.0 DMA (Direct Memory Access) Vs PIO (Programmed Input/Output)

DMA is normally used to transfer large blocks of data from one buffer to another and thus the CPU is available to perform other tasks. When an LSI chip is used to perform DMA, the information about the transfer, such as address (source and destination) of ports, byte count is first written into control registers of DMA chip. When the port address changes, the new information should be written in these registers. To emphasize this point, DMA setup time was calculated for the following two categories: i) Data transferred from a new port to RAM for each operation, ii) Data transferred from the same port and the same block length for a subsequent operation. For the purpose of this calculation, Z80 DMA architecture is used. It should be noted that after initial setup Z80 DMA transfers 1 byte in 1 μSec with CPU clock or 4MHZ:

8.0 DMA Vs PIO (continued)

i) It will take 63.5 USec (254 clock cycles) to set up DMA)+1X (no. of bytes to be transferred) μSec.

ii) After the initial setup time of 63.5 MSec, it will take 11 μSec (44 clock cycles) + 1X (no. of bytes to be transferred) μSec, the address of ports and number of bytes being transferred are identical in all subsequent operations.

Under program I/O (Ref. Table I), it takes 53.0 μSec (212 clock cycles) to transfer 6 bytes from a new port whereas for DMA under identical conditions it will take 63.5 μSec + 6 μSec = 69.5 μSec.

9.0 RELIABILITY

Reliability is calculated for individual components (Ref. Table III.) The reliability estimates in this table are provided by the Reliability Department of TRW (Space Park). From these calculations, MTBF is predicted as 315K hours.

Prediction Assumptions:

1) Class B parts
2) Current production
3) Ground benign environment
4) NMOS or TTL technology
5) Junction temperature = 50^{o}C
6) Hermetically sealed dual-in-line packages for ICs.

10.0 POWER DISSIPATION

The architecture of HSS Communication Controller (shown in the block diagram (Fig. 1) could be implemented by using i) NMOS and low power schottky components (LSTTL), ii) CMOS and LSTTL.

TABLE III

PRELIMINARY RELIABILITY PREDICTION
(One Microprocessor Architecture)

Item	Part No.	λ (failures/10^6Hr)	Qty	Total λ (failures/10^6Hr)
1	Z80ACPU	0.0526	1	0.0526
2	Z80ACTC	0.0256	1	0.0256
3	2661	0.0540	4	0.2160
4	5381-1	0.1137	2	0.2274
5	TMS 4016	0.5214	4	2.0856
6	57401	0.025	4	0.1
7	26LS32	0.0033	46	0.1518
8	26LS31	0.0033	22	0.0726
9	54LS138	0.0081	2	0.0162
10	54LS148	0.0090	1	0.0090
11	54LS174	0.0094	3	0.0282
12	54LS240	0.0117	5	0.0585
13	54LS257	0.0081	2	0.0162
14	54LS374	0.0179	2	0.0358
15	54LS00	0.0058	3	0.0174
16	54LS02	0.0058	3	0.0174
17	54LS04	0.0058	3	0.0174
18	54LS08	0.0058	3	0.0174
19	54LS32	0.0058	3	0.0174

10.0 POWER DISSIPATION (continued)

If NMOS and LSTTL components (Table IV) are used, the power dissipation is 18.66 watts (considering 70% efficiency of the power supply).

With CMOS and LSTTL components (Table V), the power dissipation is 1.54 Watts (considering 70% efficiency of the power supply). It should be noted that most of the CMOS parts are new and thus not MIL-qualified. The microprocessor NSC800 is a CMOS version of Z80 (not pin compatible).

11.0 COMSEC (Separation of Black and Red Data)

Design Description

Figure 4 represents a block diagram of the HSS communications controller utilizing dual microprocessors. The basic architecture provides for red/black data separation by division of the nodal processing functions between the two processors. In this architecture, the only path for data onto or off of the fiber optic network is via the crypto device; thus, red data would be prohibited from entering the network.

The following functions are identified for the black microprocessor:

1) Perform link level protocol
2) Provide for message buffer control
3) Provide for channel multiplexing
4) Provide interface control to crypto unit
5) Control message input and output
6) Perform Flag Test.

(The red microprocessor will perform all functions related to message processing, and interface control as shown in Figure 1. In addition, several control flags must be set by the red microprocessor to be tested by the black microprocessor. This will include specific signals enabling and disabling retransmission, channel selection, etc.)

TABLE IV

POWER DISSIPATION

(NMOS and Low Power Schottky)

Item	Component	Manufacturer	Description	Qty	Power MW
1	Z80ACPU	Zilog	CPU	1	1000
2	Z80ACTC	"	Counter Timing Circuit	1	600
3	2661	Signetics	USART	6	2500
4	5381-1	MMI	1KX8 PROM	1	950
5	TMS 4016	TI	2KX8 STATIC RAM	4	1900
6	57401	MMI	16X4 FIFO	4	3000
7	26LS32	AMD	Line Receiver	6	1560
8	26LS31	AMD	Line Driver	3	900
9	54LS138	TI	Decoder	2	68
10	54LS148	"	Priority Encoder	1	60
11	54LS174	"	Hex D-Flip Flop	3	42
12	54LS240	"	Octal Buffer	5	725
13	54LS257	"	Multiplexer	2	120
14	54LS374	"	Octal Latch	2	270
15	54LS00	"	Quad 2-input NAND	3	36
16	546502	"	Quad 2-input Nor	3	42
17	54LS04	"	Hex Inverter	3	54
18	54LS08	"	Quad 2-input AND	3	66
19	54LS32	"	Quad 2-input OR	3	74
					13.967 W

No. of ICs = 65
Estimated No. of PC Cards = 4

TABLE V

POWER DISSIPATION

(CMOS And Low Power Schottky)

Item	Component	Manufacturer	Description	Qty	Power MW
1	NSC800	National	CPU	1	69.2
2	6102	Harris Intersil	Counter Timing Circuit	1	20.0
3	6402	Harris Intersil	USART	6	60.0
4	IM6316	Intersil	2KX8 ROM	1	0.5
5	6504	Harris Intersil	4KX1 STATIC RAM	16	0.016
6	4703B	Fairchild	16X4 FIFO	4	5.0
7	DS78C20	National	Diff Receiver	23	920.0
8	78C29	"	Diff Driver	11	5.5
9	4514B	Fairchild	Decoder	2	1.5
10	54LS148	TI	Priority Encoder	1	60.0
11	40174B	Fairchild	Hex D Flip-Flop	5	3.75
12	40097B	"	Hex Buffer	8	1.2
13	4512B	"	Multiplexer	2	1.5
14	4011B	"	Quad 2-input NAND	3	1.125
15	4002B	"	Quad 2-input NOR	3	1.125
16	4049B	"	Hex inverting Buffer	3	1.125
17	4081B	"	Quad 2-input AND	3	1.125
18	4071B	"	Quad 2-input OR	3	1.125
	No. of ICs = 96			Total	1.15 Watt
	Estimated No. of PC Cards = 5				

Conclusions

The dual processor architecture needs more hardware than the one processor configuration which leads to increased costs. There is only minimal impact on the reliability and power consumption figures between the two.

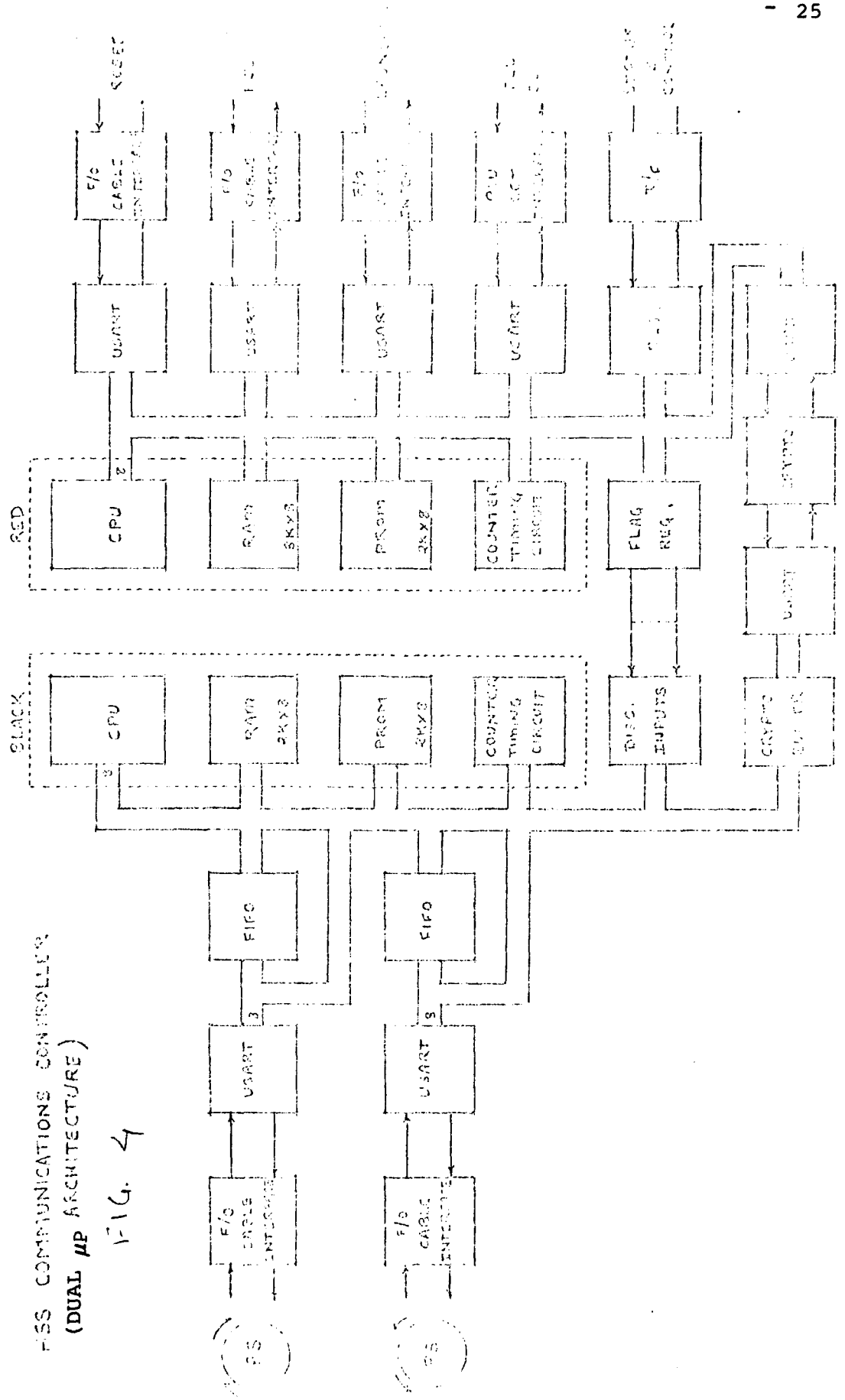

FIG. 4

FSS COMMUNICATIONS CONTROLLER
(DUAL μP ARCHITECTURE)